# PATENT ABSTRACTS OF JAPAN

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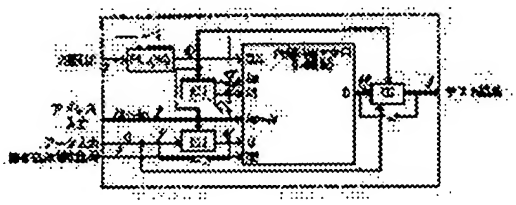
## (54) SEMICONDUCTOR STORAGE DEVICE WITH BUILT-IN HIGH SPEED SELF TESTING CIRCUIT

(57)Abstract:

PURPOSE: To reduce a testing cost and to reduce the shipping cost of an LSI by shortening the testing time of a memory LSI and diagnosing a high speed operation using of an expensive and low speed tester.

CONSTITUTION: At the time of a testing, the inside of the LSI is operated with an external multiplied frequency by providing an internal clock generating PLL for multiplying an external clock. At this time, circuits (are an AGU and a DGU respectively) generating automatically the one part of an address and a data inputting signal with an internal frequency are mounted on a device. The data inputting signal is constituted so that the signal is started by an input signal from the outside and the '0' and '1' of the signal are switched alternately with the internal frequency. Moreover, a decision circuit DC deciding whether the output signal from the internal circuit is of the alternation of '0' and '1' or not, and the output signal coincides with an expected value from the outside or not is mounted in the device. With those circuits, the memory circuit of the inside of the LSI is tested with the external multiplied frequency.



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* NOTICES *



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## DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to shortening of large-scale-izing of a semiconductor memory, and test time amount, and low cost-ization.
[0002]
[Description of the Prior Art] In the conventional semiconductor integrated circuit (LSI), when diagnosing the interior action of LSI (test), a test pattern is impressed to an input pin from the exterior, and it is carrying out by checking whether LSI outputs the result as expected value from an output pin. Especially, in Memory LSI, an addressing signal, a write-in data signal, and a write-in readout control signal are given as an input, and write-in readout actuation of the information on a memory cell is performed to all memory cells, changing an input address pattern. The example of circuitry of the conventional memory is shown in drawing 3 , and the timing chart of operation is shown in drawing 4 . In order for LSI shown in drawing 3 to diagnose the function of this LSI for the configuration which operates synchronizing with an external clock frequency (f), an input signal as shown in drawing 4 is inputted on a frequency f, and the equipment which judges an output to coincidence is needed. In order to perform the functional test of current and such LSI, the equipment of the dedication called an LSI circuit tester is used. The block diagram in the case of performing the functional diagnosis of LSI which used the LSI circuit tester for drawing 5 is shown. An LSI circuit tester has a test pattern generator, and an expected-output pattern generator and an output judging machine. The signal generated from the test pattern generator is impressed to the trial LSI-ed as an input signal, and judges good/defect examined [ LSI ] for the output signal of the from examined [ LSI ] as compared with the expected value in a circuit tester. Moreover, on the other hand, the diagnostic circuit of the LSI function which this LSI circuit tester has is built in LSI, and invention which tests the LSI itself is indicated by JP,63-184989,A using that circuit.
[0003]
[Problem(s) to be Solved by the Invention] However, the working speed more than LSI which said LSI circuit tester evaluates at least will be required. However, in order to evaluate it, the investment to a high-speed LSI circuit tester is needed with improvement in the speed and large-scale-ization of LSI in recent years, and increase of the LSI circuit tester occupancy time amount for the test of LSI has become one of the big factors which increases the shipment cost of LSI. Moreover, in recent years, since improvement in the speed of an interface circuitry with the LSI exterior does not follow to improvement in the speed of the internal circuitry of LSI, the problem that the working speed of the LSI internal circuitry which can operate at a high speed cannot be evaluated correctly is arising.
[0004] Also with a low speed circuit tester, the purpose of this invention enables a diagnosis of a high speed LSI, and realizes reduction of the shipment cost of LSI while it gathers test effectiveness and attains shortening of test time amount by preparing the auxiliary addition circuit for diagnosing the own function of LSI at a high speed in LSI.
[0005]
[Means for Solving the Problem] the circuit which carries out multiplying of the frequency of the signal with which the 1st invention is impressed from the exterior for a diagnosis of the function inside, and the circuit which compresses the output corresponding to the input signal of a frequency with which multiplying was carried out to become equal to the signal frequency of said external impression -- having -- the rate of multiplying of the signal frequency of external impression -- it is -- the interior -- it is the semiconductor memory characterized by the diagnosable thing.
[0006] Moreover, it generates as a mutual train of 1 and 0, and the data for 1 bit written in the semiconductor memory

which should diagnose the interior are made to correspond to the input signal of external impression of the initial data of the train in the circuit which carries out multiplying of the frequency of the signal made to impress from the above-mentioned exterior.

[0007] Moreover, if the initial data of the expected value to which the readout data from the semiconductor memory with which the interior should diagnose the above-mentioned output in the circuit which carries out time amount compression are the mutual train of 1 and 0, and were impressed from the exterior, and its readout signal train correspond, the signal it is supposed that it is normal actuation will be outputted.

[0008]

[Function] According to this invention, even when large-scale-izing and improvement in the speed of LSI progress further, increase of test cost can be controlled.

[0009]

[Example] Next, the example of this invention is explained with reference to drawing 1 . Drawing 1 is a circuitry Fig. in the case of testing LSI which has static memory (SRAM) as an internal circuitry. A timing chart of operation is shown in drawing 2 . An external clock (CLK) and an address input data input are given on a frequency (f). Multiplying (this example 4 times) of the clock is carried out by the phase-locked loop circuit (PLL) circuit inside LSI. Moreover, the increment of a part of address (in order to use a 4 times as many clock as this inside LSI in this example, it is a part for 2 bits of low order) is carried out by the internal address automatic incrementer (AGU) on an internal clock frequency. the case where external data are 1 as an in-house data is shown in drawing 2 -- 1-0-1- in the case of 0 and 0, it writes in with 0-1-0-1, and it is the data generating circuit DGU and is automatically generated on an internal frequency. These input signals are impressed to the SRAM macro inside LSI, and the test of an LSI internal circuitry is performed by multiplying of an external frequency. In the output-value comparison compression circuit DC, between the expectation value pattern (if it is 1 1-0-1- if it is 0 and 0 0 -1 -0 -1) given from the outside, and a multiplying period, a sequential comparison is carried out, output data are the mutual trains of 0 and 1, and output data judge whether the initial data are in agreement with expected-value data, and output the result on an external frequency. In this example, since the internal clock doubled four among one period of an external clock can perform four memory actuation, test time amount can be set to one fourth in conventional. Moreover, the I/O circuit of LSI becomes diagnosable from an external clock frequency over a low speed I/O circuit about the internal circuitry in which high-speed operation is more possible in order just to operate with an external clock. Furthermore, a diagnosis of a high speed LSI is attained also with a low speed circuit tester. For example, a diagnosis of the high speed LSI of 200MHz actuation is attained also with a circuit tester with cheap 50MHz actuation extent.

[0010] Two or more memory cell blocks are activated for this invention to coincidence, two or more bits are read to coincidence, and the test effectiveness of LSI improves further by combining with the conventional multi-bit parallel test technique of detecting coincidence of those results.

[0011]

[Effect of the Invention] The purpose of enabling a diagnosis of a high speed LSI and realizing reduction of the shipment cost of LSI also with a low speed circuit tester is attained by the effectiveness of this invention while it gathers test effectiveness and attains shortening of test time amount by the configuration indicated to the claim.

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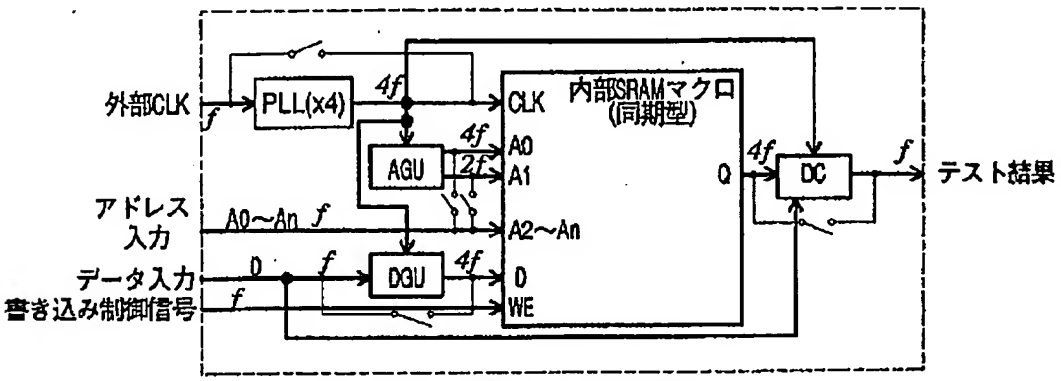
[Translation done.]

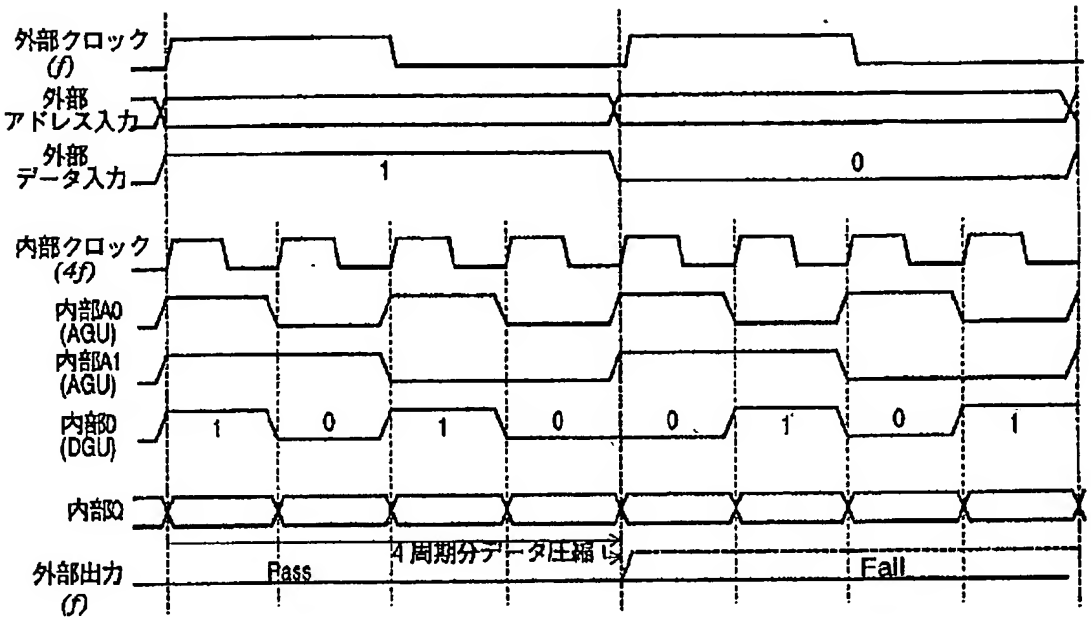
Drawing selection drawing 1




PLL(x4):PLL 4倍クロック発生回路
AGU:2bitアドレス自動インクリメンタ
DGU:書き込みデータ発生回路
DC:4周期データ圧縮比較回路

[Translation done.]

Drawing selection drawing 2

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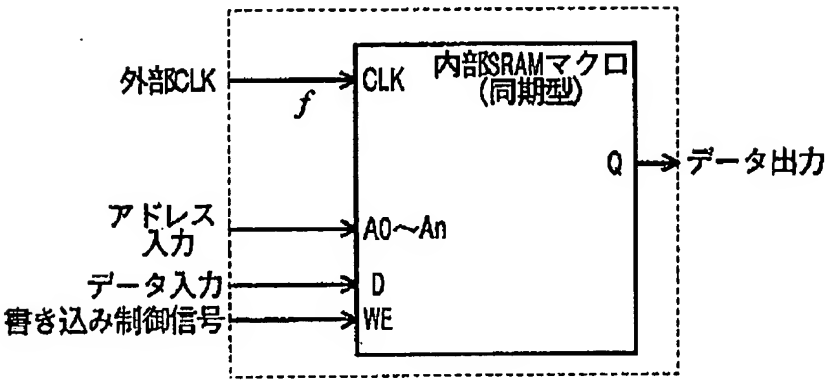
CLAIMS

[Claim(s)]
[Claim 1] the circuit which carries out multiplying of the frequency of the signal impressed from the exterior for a diagnosis of the function inside, and the circuit which compresses the output corresponding to the input signal of the frequency by which multiplying was carried out to become equal to the signal frequency of said external impression -- having -- the rate of multiplying of the signal frequency of external impression -- the interior -- the semiconductor memory characterized by the diagnosable thing.
[Claim 2] The semiconductor memory according to claim 1 characterized by generating as a mutual train of 1 and 0 and making the data for 1 bit written in the semiconductor memory which should diagnose the interior in the circuit which carries out multiplying of the frequency of the signal made to impress from the above-mentioned exterior correspond to the input signal of external impression of the initial data of the train.
[Claim 3] The semiconductor memory according to claim 1 with which the readout data from the semiconductor memory with which the interior should diagnose the above-mentioned output in the circuit which carries out time amount compression are the mutual train of 1 and 0, and are characterized by outputting the signal it is supposed that it is normal actuation if the initial data of the expected value impressed from the exterior and its readout signal train correspond.

[Translation done.]

Drawing selection drawing 3

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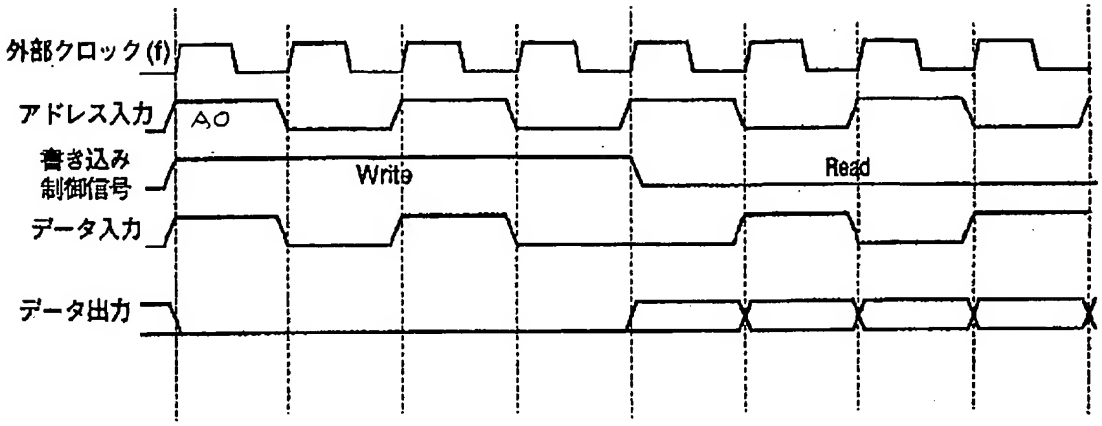
Drawing selection drawing 4

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